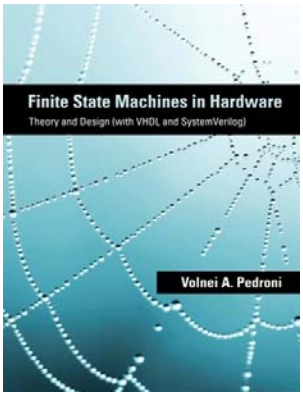

Finite State Machines in Hardware: Theory and Design (with VHDL and System Verilog)

Volnei A. Pedroni

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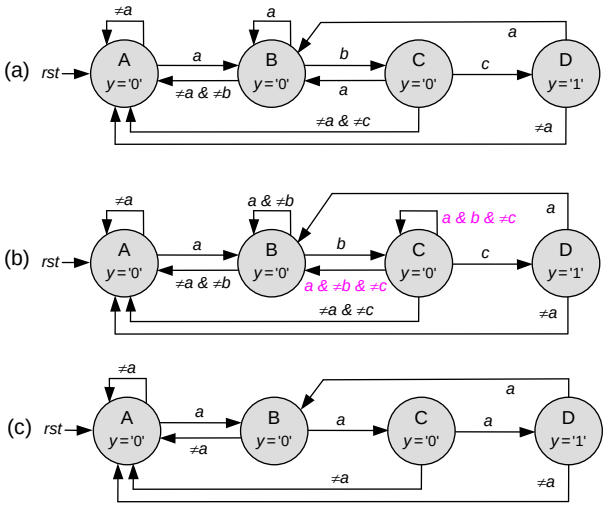
Errata

(rev. 1)

Page 95: Corrections in figure 5.14b, as shown below. (Collaborated by Timothy Sttots)



Page 102: At the end of exercise 5.14, replace “8.11” with “8.9”.

Page 111: State-encoding for Quartus Prime and Vivado are detailed in section “9.5.1 State Machine Encoding Attributes” of the VHDL book (Circuit Design with VHDL); in summary:

Vivado: *fsm_encoding*
Options: "sequential", "one_hot", "gray", "johnson", and "auto" (default).

Quartus Prime: *syn_encoding*
Options: sequential", "one-hot", "gray", "johnson", "compact" (minimal bits), "auto" (default), and user-encoded.

Page 173: At the beginning of section 8.11.10, replace “king” with “kind”.

Page 254: In the caption of figure 12.2, replace “11.14d” with “11.14c”.

Pages 255-256: In lines 65 and 67, replace “*y*(*i*-1)” with “*y*(*i_reg*)”.