Appendix I: VGA Video Interface

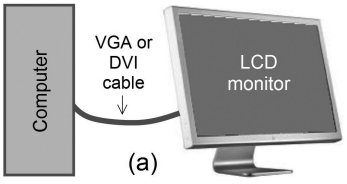
1. VGA Interface

The original video graphics array (VGA) interface was introduced by IBM in 1987 for connecting computers to analog cathode ray tube (CRT) video monitors. Many other versions were introduced subsequently (figure I.1b), which were collectively called "VGA modes." Traditional monitors were replaced with liquid crystal display (LCD) monitors (figure I.1a), which allow for a fully digital operation (the interface is then called digital visual interface or DVI as described in appendix J, instead of VGA). However, most still support VGA interfacing, which is much simpler than DVI, so it is a good place to start when one wants to learn about video drivers.

A major specification of a video monitor is its number of pixels, counted as indicated in figure I.1c. As shown in figure I.1b, the resolution of the original VGA standard is 640 × 480, while 1920 × 1080 (Full HD, listed in appendix J) is currently the most common option.

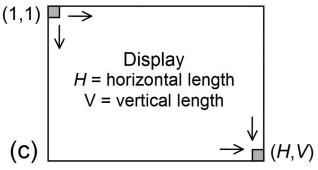
2. General VGA Interface Architecture

Figure I.2 depicts the general architecture of VGA systems, with the graphics controller (computer side) divided in three parts, as follows.



(b)

Name	Pixels (*H* x *V*)	Aspect ratio
VGA	640 x 480	4:3
SVGA	800 x 600	4:3
XGA	1024 x 768	4:3
SXGA	1280 x 1024	5:4



(c)

Figure I.1
(a) VGA (analog video) or DVI (digital video) cable; (b) Some members of the VGA family; (c) Pixel count.

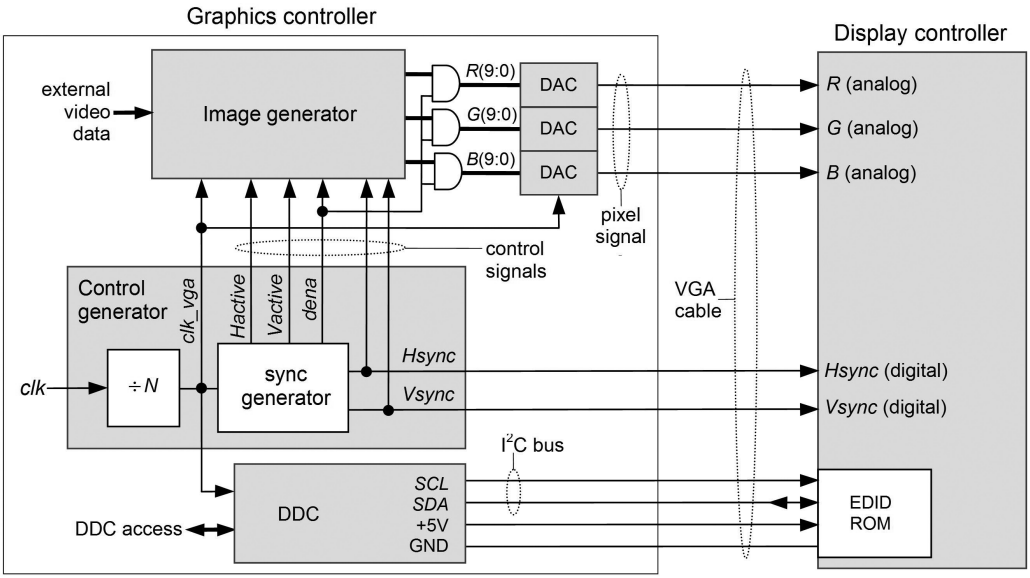


Figure I.2
VGA interface architecture.

Image generator: Produces the pixel signals (*R*, *G*, *B*), which are converted to analog voltages between 0V and 0.7V by the DACs (usually with a resolution between 6 and 10 bits) before being sent to the monitor. These signals obviously vary from one application to another.

Control signals generator: Produces the VGA clock, *clk_vga*, plus the actual control signals of *Hactive* (horizontal active window), *Vactive* (vertical active window), *dena* (display enable), *Hsync* (horizontal sync), and *Vsync* (vertical sync). This block is application-independent (it depends only on the VGA mode), so its design is always the same.

DDC (Display Data Channel): Allows the computer to read the display's features (supported resolutions, timings etc.), stored in a ROM with extended display identification data (EDID) format. The original VGA mode ($640 \times 480 \times 60$Hz) is supported by any monitor by default. Notice that this communication employs the I^2C protocol (appendix G). This block too is application-independent.

Hsync and *Vsync* are responsible for determining when a new line or a new frame should start, respectively, with their timings defining the VGA mode. *Hactive* and *Vactive* represent the time intervals during which an image is actually being drawn on the screen. Finally, *dena* is responsible for turning the pixel signals off during retrace, so it can be obtained by simply ANDing *Hactive* and *Vactive*. Note that only two of the five control signals are transmitted to the monitor.

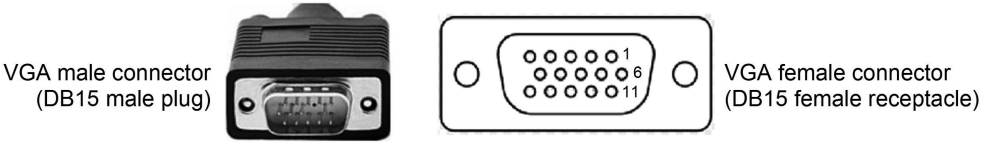
3. VGA Connector

Figure I.3 shows a VGA connector and its pins. There are five main signals, sent out through pins 1–3 and 13–14. Wires 1 to 3 transmit the color signals (*R*, *G*, *B*) to the monitor, which are analog voltages between 0V and 0.7V on two parallel 75Ω resistors (all other signals are digital), while wires 13–14 transmit the horizontal and vertical synchronism signals (*Hsync*, *Vsync*). The reader is invited to compare these pins to the wires in figure I.2.

4. Construction of Control Signals

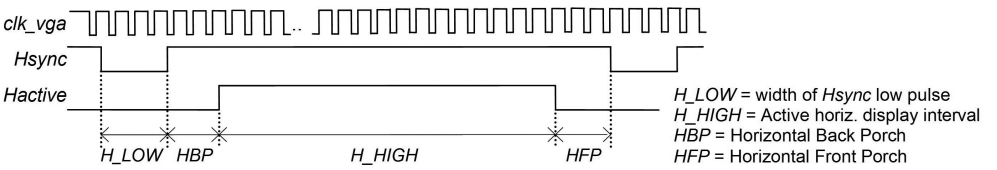
Figure I.4 shows the specifications for several VGA modes. It shows also the waveforms for *Hsync* and *Hactive* (based on *clk_vga*), which consist of four parts (all measured in number of pixels; i.e., number of clock cycles), called *H_LOW* (width of the horizontal synchronization pulse), *HBP* (horizontal back porch), *H_HIGH* (active line display interval), and *HFP* (horizontal front porch).

The vertical time diagram is depicted in figure I.5, also consisting of four parts (all measured in number of lines; i.e., number of *Hsync* cycles), called *V_LOW* (width of the vertical



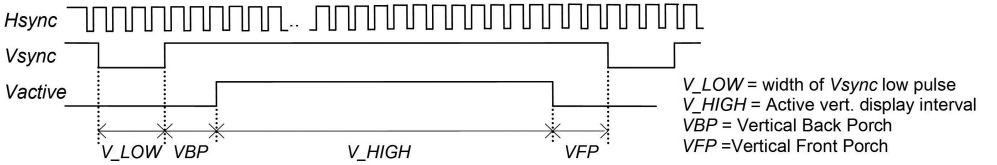
Pin	Signal	Direction	Simplest setup
1	*R* (analog red, 0V-0.7V on 37.5Ω)	To monitor	Connected (analog)
2	*G* (analog green, 0V-0.7V or 0.3V-1V on 37.5Ω)	To monitor	Connected (analog)
3	*B* (analog blue, 0V-0.7V on 37.5Ω)	To monitor	Connected (analog)
4	ID2	From monitor	N/C
5	GND (general and for +5V)	To monitor	GND
6	GND for *R*	To monitor	GND
7	GND for *G*	To monitor	GND
8	GND for *B*	To monitor	GND
9	No pin or +5V (optional)	To monitor	N/C
10	GND for *Hsync* and *Vsync*	To monitor	GND
11	ID0	From monitor	N/C
12	*SDA* (for I^2C interface)	Bidirectional	N/C
13	*Hsync* (horizontal sync, 0V/5V waveform)	To monitor	Connected (digital)
14	*Vsync* (vertical sync, 0V/5V waveform)	To monitor	Connected (digital)
15	*SCL* (for I^2C interface)	To monitor	N/C

Figure I.3
VGA connector.



VGA mode		Refresh rate (Hz)	Clock (MHz)	Horizontal timing (in clock pulses, same as pixels)				
Name	Resolution (*H* x *V*)			*H_LOW* (pixels)	*HBP* (pixels)	*H_HIGH* (pixels)	*HFP* (pixels)	Total pixels
VGA	640 x 480	60	25	96	48	640	16	800
VGA	640 x 480	75	36	96	48	640	16	800
SVGA	800 x 600	60	40	128	88	800	40	1056
SVGA	800 x 600	75	50	80	160	800	16	1056
XGA	1024 x 768	60	65	136	160	1024	24	1344
SXGA	1280 x 1024	60	108	112	248	1280	48	1688

Figure I.4
Examples of VGA modes and corresponding horizontal time parameters.



VGA mode		Refresh rate (Hz)	Clock (MHz)	Vertical timing (in lines, same as *Hsync* pulses)				
Name	Resolution (*H* x *V*)			*V_LOW* (lines)	*VBP* (lines)	*V_HIGH* (lines)	*VFP* (lines)	Total lines
VGA	640 x 480	60	25	2	33	480	10	525
VGA	640 x 480	75	32	2	33	480	10	525
SVGA	800 x 600	60	40	4	23	600	1	628
SVGA	800 x 600	75	50	3	21	600	1	625
XGA	1024 x 768	60	65	6	29	768	3	806
SXGA	1280 x 1024	60	108	3	38	1024	1	1066

Figure I.5
Examples of VGA modes and corresponding vertical time parameters.

synchronization pulse), *VBP* (vertical back porch), *V_HIGH* (active column display interval), and *VFP* (vertical front porch).

For example, in the $640 \times 480 \times 60$Hz VGA option, the drawing of one line takes 800 cycles of *clk_vga* (figure I.4), while one frame requires a time equivalent to 525 lines (figure I.5). Consequently, to be able to generate 60 frames per second, the frequency of *clk_vga* must be $800 \cdot 525 \cdot 60 \approx 25$MHz (the original value is 25.175MHz, for a refresh rate of 59.94Hz, inherited from the National Television System Committee [NTSC] television system).

A complete implementation example is presented in example 17.6.