# **Appendix M: List of Enumerated Examples and Exercises**

### Chapter 6. Code Structure and Composition

#### Examples

- Example 6.1. Parity detector
- Example 6.2. D-type flip-flop (DFF)
- Example 6.3. Registered add-and-compare circuit

### **Chapter 7. Predefined Data Types**

### Examples

Example 7.1. Tri-state buffer

Example 7.2. Circuit with "don't care" values

Exercises

Exercise 7.1. Required packages

Exercise 7.2. Possible data types

- Exercise 7.3. Number of bits and decimal values
- Exercise 7.4. Legal versus illegal aggregations

Exercise 7.5. Legal versus illegal concatenations

Exercise 7.6. Resizing unsigned and signed data

Exercise 7.7. Resizing signed and standard-logic data

Exercise 7.8. Resizing fixed-point data

Exercise 7.9. Resizing floating-point data

Exercise 7.10. Type conversion (1)

Exercise 7.11. Type conversion (2)

- Exercise 7.12. Strength-stripping functions
- Exercise 7.13. Type qualification (1)

Exercise 7.14. Type qualification (2)

## Chapter 8. User-Defined Data Types

### Examples

Example 8.1. Multiplexer with a user-defined input type

Example 8.2. Vector-matrix multiplier with user-defined types

### Exercises

Exercise 8.1. Dimensionality of data arrays

Exercise 8.2. User-defined 1D×1D array types

Exercise 8.3. User-defined 2D array types

Exercise 8.4. User-defined 1D×1D×1D array types

- Exercise 8.5. Legal versus illegal assignments (1)
- Exercise 8.6. Legal versus illegal assignments (2)
- Exercise 8.7. Checking whether a data array contains only zeros
- Exercise 8.8. Setting all elements of a data array to zero
- Exercise 8.9. Checking arrays of integers
- Exercise 8.10. Resetting arrays of integers
- Exercise 8.11. Checking whether an integer is odd

# Chapter 9. Operators and Attributes

### Example

Example 9.1. Delay line built with attribute keep

Exercises

- Exercise 9.1. Logical operators (1)
- Exercise 9.2. Logical operators (2)
- Exercise 9.3. Logical operators (3)
- Exercise 9.4. Arithmetic operators (1)
- Exercise 9.5. Arithmetic operators (2)
- Exercise 9.6. Arithmetic operators (3)
- Exercise 9.7. Comparison operators (1)

Exercise 9.8. Comparison operators (2) Exercise 9.9. Comparison operators (3) Exercise 9.10. Shift and concatenation operators Exercise 9.11. Attributes of array type and objects Exercise 9.12. State machine encoding (1) Exercise 9.13. State machine encoding (2) Exercise 9.14. Binary-to-BCD conversion

### Chapter 10. Concurrent Code

#### Examples

Example 10.1. Priority encoder

Example 10.2. Conditional adder instantiation

Example 10.3. Carry-ripple adder built with full-adder components

Example 10.4. Hamming-weight calculator

Example 10.5. Signed integer adder

Example 10.6. Floating-point adder and multiplier

### Chapter 11. Concurrent Code: Practice

#### Examples

Example 11.1. Vectors absolute difference calculator

Example 11.2. Programmable combinational delay line (structural)

Example 11.3. Sine calculator with integers and ROM-type memory

#### Exercises

Part 1: Combinational Logic Circuits

Exercise 11.1. Multiplexer (1)

Exercise 11.2. Multiplexer (2)

Exercise 11.3. Address decoder

Exercise 11.4 Leading-ones counter

Exercise 11.5: Largest cluster of ones

Exercise 11.6. Circuit with "don't care" outputs

Exercise 11.7. Binary-to-BCD converters

Exercise 11.8. Ring oscillator

#### Part 2: Combinational Arithmetic Circuits

- Exercise 11.9. Unsigned and signed integer multipliers
- Exercise 11.10. Unsigned and signed integer dividers
- Exercise 11.11. Overflow analysis in division of integers
- Exercise 11.12. Division of integers with rounding
- Exercise 11.13. Floating-point adder and multiplier
- Exercise 11.14. Floating-point subtracter and divider
- Exercise 11.15. Generic chain-type adder array
- Exercise 11.16. Generic tree-type adder array
- Exercise 11.17. Multiple detector
- Exercise 11.18. Square-root calculator

### Chapter 12. Sequential Code

#### Examples

- Example 12.1. Flip-flop inference with and without sensitivity list
- Example 12.2. Consequences of incomplete sensitivity lists
- Example 12.3. Counter with is\_max flag and RTL analysis
- Example 12.4. Counters with signal and variable
- Example 12.5. Timer with BCD outputs
- Example 12.6. Counter with is\_max flag implemented with variable
- Example 12.7. Flip-flop with *q* and *qbar* outputs
- Example 12.8. Registered adder
- Example 12.9. Shift register with odd implementations
- Example 12.10. Recommended shift register implementation
- Example 12.11. Leading-ones counter with combinational loop

### **Chapter 13. Sequential Code: Practice**

#### Examples

- Example 13.1. Generic tree-type adder array
- Example 13.2. Single-switch debouncer
- Example 13.3. FIR filter with fixed coefficients
- Example 13.4. Sequential square-root calculator

#### Exercises

- Part 1: Signal versus Variable
- Exercise 13.1. Guess the circuit (1)
- Exercise 13.2. Guess the circuit (2)
- Exercise 13.3. Guess the circuit (3)
- Part 2: Combinational Circuits
- Exercise 13.4. Hamming-weight calculator
- Exercise 13.5. Largest cluster of ones
- Exercise 13.6. Generic chain- and tree-type maximum detector
- Part 3: Counters and Clock Dividers
- Exercise 13.7. Counter with failure flag
- Exercise 13.8. Counter with *is\_max* flag
- Exercise 13.9. Direct and reversed gray counters
- Exercise 13.10. Clock divider by any integer with symmetric phase
- Exercise 13.11. Clock divider by odd integer with positive-edge-only flip-flops
- Part 4: Timers and Associated Circuits
- Exercise 13.12. Single-switch debouncer with a test circuit
- Exercise 13.13. Simplified single-switch debouncer
- Exercise 13.14. Multi-input debouncer for non-concurrent switches
- Exercise 13.15. Multi-input debouncer for independent switches
- Exercise 13.16. Multi-switch debouncer with clock gating
- Exercise 13.17. Pulse width modulator (PWM)
- Exercise 13.18. Timer (1)
- Exercise 13.19. Timer (2)
- Exercise 13.20. Kitchen timer (1)
- Exercise 13.21. Kitchen timer (2)
- Part 5: Synchronism
- Exercise 13.22. One-shot and pulse-capture circuits
- Exercise 13.23. Pulse stretcher
- Exercise 13.24. Frequency meter
- Exercise 13.25. Measuring the width of asynchronous pulses

- Part 6: Shifters
- Exercise 13.26. Tapped delay line
- Exercise 13.27. Pseudo-random sequence generator
- Exercise 13.28. Continuously shifting display
- Part 7: Controllers
- Exercise 13.29. Reference-value generator
- Exercise 13.30. Air conditioning controller
- Exercise 13.31. PWM breathing effect
- Exercise 13.32. Quick-finger game
- Part 8: Serial Arithmetic Circuits
- Exercise 13.33. Serial absolute difference between two vectors calculator
- Exercise 13.34. Moving-average calculator
- Exercise 13.35. Determining the variance of video frames

Part 9: Filters

- Exercise 13.36. FIR filter with underlimited data path
- Exercise 13.37. FIR filter with programmable coefficients
- Exercise 13.38. IIR filter with transposed direct form I architecture
- Part 10: With Component Instantiation (Structural Code)
- Exercise 13.39. Modular counter (structural code)
- Exercise 13.40. Debouncer with a test circuit (structural code)
- Exercise 13.41. Frequency meter (structural code)
- Exercise 13.42. Tapped delay line (structural code)
- Exercise 13.43. Air conditioning controller (structural code)
- Exercise 13.44. PWM breathing effect (structural code)

### Chapter 14. Packages and Subprograms

#### Examples

- Example 14.1. Package with function
- Example 14.2. Function *ceil\_log2* in a package
- Example 14.3. Function *ceil\_log2* in an architecture
- Example 14.4. Function *slv\_to\_integer* in a process
- Example 14.5. Function *binary\_to\_bcd*
- Example 14.6. Procedure *find\_min\_and\_max*

#### Exercises

Exercise 14.1. Function *binary\_to\_bcd* Exercise 14.2. Function *integer\_to\_slv* Exercise 14.3. Function *integer\_to\_onehot* Exercise 14.4. Function *leading\_ones* Exercise 14.5. Function *leading\_weight* Exercise 14.6. Function *sort\_binary* Exercise 14.7. Function *sla* for std\_ulogic\_vector (overloaded operator) Exercise 14.8. Procedure *find\_min\_and\_max* Exercise 14.9. Procedure *equalize\_lengths* Exercise 14.10. Procedure *add\_signed* Exercise 14.11. Procedure *mean\_median* 

### Chapter 15. The Case of State Machines

### Exercises

Exercise 15.1. Checking the templates for regular (category 1) machines Exercise 15.2. Checking the templates for timed (category 2) machines Exercise 15.3. Checking the templates for recursive (category 3) machines

### Chapter 16. The Case of State Machines: Practice

#### Examples

Example 16.1. ASCII-sequence detector Example 16.2. Garage door controller Example 16.3. Password decoder Example 16.4. SPI interface for an A/D converter Example 16.5. SRAM memory interface Example 16.6. Datapath controller for a serial multiplier Exercises Part 1: Exercises with Regular FSMs Exercise 16.1. Checking the templates for regular (category 1) machines Exercise 16.2. Manchester encoder Exercise 16.3. Flag monitor Part 2: Exercises with Timed FSMs
Exercise 16.4. Checking the templates for timed (category 2) machines
Exercise 16.5. Pulse stretcher
Exercise 16.6. Multi-input debouncer for non-concurrent switches
Exercise 16.7. Playing with a seven-segment display
Exercise 16.8. Residential alarm system
Exercise 16.9. Residential alarm system with buzzer
Part 3: Exercises with Recursive FSMs
Exercise 16.10. Checking the templates for recursive (category 3) machines
Exercise 16.11. Reference-value definer with embedded debouncer (a recursive timed FSM)
Exercise 16.12. SRAM interface

### **Chapter 17. Additional Design Examples**

### Examples

Example 17.1. SPI interface for an EEPROM device (with FSM)

Example 17.2. SPI interface for an EEPROM device (with pointer)

Example 17.3. I<sup>2</sup>C interface for an A/D converter (with pointer)

Example 17.4. I<sup>2</sup>C interface for an A/D converter (with pointer built with FSM)

Example 17.5. Digital watch with liquid crystal display

Example 17.6. VGA video interface for a hardware-generated image

Example 17.7. DVI video interface for a hardware-generated image

Example 17.8. TMDS 8B/10B encoder

#### Exercises

Part 1: Exercises with SPI Protocol

Exercise 17.1. SPI interface for an A/D converter

Exercise 17.2. SPI interface for a temperature sensor

Exercise 17.3. SPI interface for an accelerometer

Part 2: Exercises with I<sup>2</sup>C Protocol

Exercise 17.4. I<sup>2</sup>C interface for an A/D converter

Exercise 17.5. I<sup>2</sup>C interface for an EEPROM

Exercise 17.6. I<sup>2</sup>C interface for a temperature sensor

Exercise 17.7. I<sup>2</sup>C interface for an accelerometer

Exercise 17.8. I<sup>2</sup>C interface for a real-time clock (RTC) *Part 3: Exercises with Alphanumeric LCD*Exercise 17.9. Digital watch with LCD display (pointer-based implementation)
Exercise 17.10. Blinking "VHDL" word
Exercise 17.11. Display your name on an alphanumeric LCD *Part 4: Exercises with VGA Video Driver*Exercise 17.12. Hardware-generated image with VGA monitor (banner)
Exercise 17.14. Digital clock with VGA monitor
Exercise 17.15. Display your picture on a VGA monitor *Part 5: Exercises with DVI Video Driver*Exercise 17.16. Hardware-generated image with DVI monitor (banner)
Exercise 17.17. Bardware-generated image with DVI monitor (banner)
Exercise 17.16. Hardware-generated image with DVI monitor (banner)
Exercise 17.17. Hardware-generated image with DVI monitor (banner)
Exercise 17.19. Digital clock with DVI monitor

### Chapter 18. Introduction to Simulation with Testbenches

#### Examples

- Example 18.1. Stimuli generator
- Example 18.2. Binary-to-gray converter (a combinational circuit)
- Example 18.3. Registered multiplexer (a sequential circuit)
- Example 18.4. Binary-to-gray converter (using data files)

#### Exercises

- Exercise 18.1. Signed adder
- Exercise 18.2. Sine calculator
- Exercise 18.3. Sequential square-root calculator
- Exercise 18.4. Pulse width modulator (PWM)